PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Brian M. Shirley et al.	)	Examiner: Trong Phan
	)	
Serial No.: 09/809,586	)	Group Art Unit: 2827
	)	
Filed: March 15, 2001	)	Docket: 303.724US1
For: MULTI-BANK MEMORY	)	
	)	

APPEAL BRIEF UNDER 37 CFR § 41.37

Mail Stop Appeal Brief- Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Appeal Brief is presented in support of the Notice of Appeal to the Board of Patent Appeals and Interferences, filed on May 31, 2005, from the Final Rejection of claims 1-12 and 14-60 of the above-identified application, as set forth in the Final Office Action mailed on February 28, 2005.

The Commissioner of Patents and Trademarks is hereby authorized to charge Deposit Account No. 19-0743 in the amount of 500.00 which represents the requisite fee set forth in 37 C.F.R. § 41.2(b)(2).

This response is accompanied by a Petition, as well as the appropriate fee, to obtain a four-month extension of the period for responding to the Notice of Appeal filed May 31, 2005, thereby moving the deadline for response from July 31, 2005 to November 30, 2005.

The Appellants respectfully request consideration and reversal of the Examiner's rejections of pending claims.

APPEAL BRIEF UNDER 37 C.F.R. § 41.37

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1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the assignee, MICRON TECHNOLOGY, INC.

2. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant that will have a bearing on the Board's decision in the present appeal.

3. STATUS OF THE CLAIMS

The present application was filed on March 15, 2001 with claims 1-56. A non-final Office Action was mailed June 11, 2002, which rejected all pending claims 1-56. A non-final Office Action was mailed November 15, 2002, which rejected all pending claims 1-56. In a response to the November 15, 2002 Office Action, Appellant maintained claims 1-56 and added claims 57-60. A final Office Action was mailed March 20, 2003, which rejected all pending claims 1-60.

A Request for Continued Examination was filed on August 20, 2003 along with an amendment and response to the final Office Action which maintained claims 1-12 and 14-60, some of which were amended, and withdrew claim 13 from consideration. A non-final Office Action was mailed December 12, 2003, which rejected all pending claims 1-12 and 14-60. Appellant subsequently amended claims 1, 5, 9, and 18 on March 12, 2004. A final Office Action was mailed April 5, 2004 rejecting all pending claim 1-12 and 14-60. ON July 6, 2004 Appellant filed and amendment and response which maintained claims 1-12 and 14-60 with amendment to claims 1-2, 4-9, 14, 16, 18, 20, 22-24, 26-29, 31, 33-36, 38, 40-43, 46, 49, 52, 55, and 57-60.

A Request for Continued Examination was filed on August 5, 2004 with a request to consider the July 6, 2004 amendment and response. A non-final Office Action was mailed September 8, 2004 rejection claims 1-12 and 14-60. A final Office Action (hereinafter "the Final Office Action") was mailed February 28, 2005 rejecting claims 1-12 and 14-60.

Claims 1-12 and 14-60 stand at least twice rejected, remain pending, and are the subject of the present appeal.

4. STATUS OF AMENDMENTS

No amendments have been made subsequent to the Final Office Action dated February 28, 2005.

5. SUMMARY OF CLAIMED SUBJECT MATTER

The present subject matter relates generally to memory devices, and in particular, to memory devices having multiple banks. One embodiment illustrated in FIG. 3 (Attached as Exhibit A) provides a memory device 300. The memory device 300 includes a plurality of memory banks Bank 0, Bank 1, Bank 2, Bank 3, Bank n, Bank n-1 arranged in rows 370 372, 374 (strips) and columns 302, 304, 306, 308. The memory banks include a plurality of memory core blocks 320, 330, 331, 308, 324, 334, 328, 338. *See* FIG. 3; *see* page 5, lines 19-25.

The all memory core blocks from a first memory bank, such as memory core blocks 320 and 331 of Bank 0, and all memory core block from a second memory bank, such as memory core blocks from memory bank 1 including memory core block 330, are included a row (strip), such as strip 370. *See* FIG. 3; *see* page 5, lines 26-29. Each row in memory device 300 includes memory cores from two banks interleaved together. *Id.* For example, strip 370 includes memory cores from Bank 0 and Bank 1 alternating across the strip. *Id.* Also for example, strip 372 includes memory cores from Bank 2 interleaved with memory cores from Bank 3. *Id.*

Each row includes sense amplifiers that are shared between two banks of memory cores. Page 6, lines 1-4. For example, sense amplifiers 340 and 346 are shared between memory cores in Bank 0 and memory cores in Bank 1, and sense amplifiers 342 and 348 are shared between memory cores in Bank 2 and memory cores in Bank 3. *Id.*

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1-12 and 14-60 were rejected under 35 U.S.C. 112, first paragraph for allegedly failing to comply with the enablement requirement.

2. Claims 1-12 and 14-60 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Appellant's prior art FIG. 1 (attached as Exhibit A).

7. ARGUMENT

A. Applicable Law

1. 35 U.S.C. § 112, first paragraph

With respect to 35 U.S.C. § 112, first paragraph, the specification in an application need only describe the invention to one of ordinary skill in the art. As explained by the Federal Circuit:

> Requiring inclusion in the patent of known scientific/technological information would add an imprecise and open-ended criterion to the content of patent specifications, could greatly enlarge the content of patent specifications and unnecessarily increase the cost of preparing and prosecuting patent applications, and could tend to obfuscate rather than highlight the contribution to which the patent is directed. A patent is not a scientific treatise, but a document that presumes a readership skilled in the field of the invention. *Ajinomoto Co., Inc. v. Archer-Daniels-Midland Co.* 56 USPQ 2d 1332, 1338 (Fed. Cir. 2000).

M.P.E.P. § 2164 et seq. notes that the burden is on the Examiner to establish a *prima facie* case to maintain a rejection of non-enablement with respect to the disclosure of a patent application under 35 U.S.C. § 112, first paragraph. Such a case requires:

1. a rational basis as to
    a. why the disclosure does not teach, or
    b. why to doubt the objective truth of the statements in the disclosure that purport to teach;
2. the manner and process of making and using the invention;
3. that correspond in scope to the claimed invention;
4. to one of ordinary skill in the pertinent technology;
5. without undue experimentation; and
6. dealing with subject matter that would not already be known to the skilled person as of the filing date of the application.

"The Examiner must provide evidence ... supporting each of these elements for a rejection under the first paragraph of § 112 to be proper." See *Patent Prosecution,*

Practice and Procedure Before The United States Patent Office, Ira H. Donner, pg. 691, 2002.

Further, it should be noted that "35 U.S.C. 112 requires the specification to be enabling only to a person "skilled in the art to which it pertains, or with which it is most nearly connected. ... The specification need not disclose what is well-known to those skilled in the art and preferably omits that which is well-known to those skilled and already available to the public." *In re Buchner*, 929 F.2d 660, 661, 18 USPQ2d 1331, 1332 (Fed. Cir. 1991); *Hybritech, Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 1384, 231 USPQ 81, 94 (Fed. Cir. 1986), *cert. denied*, 480 U.S. 947 (1987); and *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1463, 221 USPQ 481, 489 (Fed. Cir. 1984)."

2. 35 U.S.C. § 103(a)

In rejecting claims under 35 U.S.C. § 103, the Examiner bears the initial burden of establishing a *prima facie* case of obviousness. *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ 1443, 1444 (Fed. Cir. 1992). *See also In re Piasecki*, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984). The Examiner can satisfy this burden by showing that some objective teaching in the prior art or knowledge generally available to one of ordinary skill in the art suggests the claimed subject matter. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Only if this initial burden is met does the burden of coming forward with evidence or argument shift to the Appellants. *Oetiker*, 977 F.2d at 1445, 24 USPQ at 1444. *See also Piasecki*, 745 F.2d at 1472, 223 USPQ at 788.

When determining obviousness, "the [E]xaminer can satisfy the burden of showing obviousness of the combination 'only by showing some objective teaching in the prior art or individual to combine the relevant teachings of the references". *In re Lee*, 277 F.3d 1338, 1343, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002), citing *In re Fritch*, 972 F.2d 1260, 1265, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992). "Broad conclusory statements regarding the teaching of multiple references, standing alone, are not 'evidence." *In re Dembiczak*, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617. "Mere denials

and conclusory statements, however, are not sufficient to establish a genuine issue of material fact." *Dembiczak*, 175 F.3d at 999, 50 USPQ2d at 1617, citing *McElmurry v. Arkansas Power & Light Co.*, 995 F.2d 1576, 1578, 27 USPQ2d 1129, 1131 (Fed. Cir. 1993).

The Federal Circuit states that, "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner doe not make the modification obvious unless the prior art suggested the desirability of the modification." *In re Fritch*, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-83 n.14 (Fed. Cir. 1992), citing *In re Gordon*, 733 F.2d 900, 902, 221 USEQ 1125, 1127 (Fed. Cir. 1984). In addition, the court stated in *In re Lee*, 277 F.3d 1338, 1343, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002), that when making an obviousness rejection based on combination, "there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by Applicant" (quoting *In re Dance*, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998).

B. The subject matter of claims 1-12 and 14-60 as described in the specification enables one skilled in the art to make and use the same as required by 35 U.S.C. § 112, first paragraph.

Claims 1-12 and 14-60 were rejected under 35 U.S.C. § 112, first paragraph, as lacking adequate enablement. Applicant respectfully traverses.

In the Final Office Action the Examiner stated that he did not understand the feature of "the first and second banks interleaved in each row in an alternating fashion" as recited in claims 1-12 and 14-60 and cannot see this in the drawings of the present patent application. This rejection has been carried through from the beginning of the extensive record of prosecution of the present patent application and the telephonic interview between Appellant's representative, Suneel Arora, and the Examiner on June 24, 2004, was an attempt to explain this feature to the Examiner. In the Final Office Action, the Examiner further stated:

> It is not understood the feature of "the first and second banks interleaved in each row in an alternating fashion" as recited in claims 1-12 and 14-60

> since it is not seen in the drawings of the present invention. Even if newly amended Fig. 3 of the present invention does show that bank 0 and bank 1 are separately connected in each row through the dash lines only which does not clearly seen to show the feature of "the first and second banks interleaved in each row in an alternating fashion" as recited in claims 1-12 and 14-60 since it is not seen in the drawings of the present invention. Furthermore, newly amended Fig. 3 still does not show bank 0 and bank 1, therefore, all banks are seen to be the same.

(Office Action ¶ 3.) However, the top row of FIG. 3 (from right-to-left) clearly shows Bank 0, Bank 1, Bank 0, Bank 1, Bank 0, Bank 1, etc. blocks interleaved in alternating fashion. (FIG. 3 is attached as Exhibit B). Therefore, Applicant respectfully submits that FIG. 3 of the present specification clearly enables any claims reciting that blocks from such Banks are "interleaved," "alternating," "every other," or similar language. That is, Bank 0 and Bank 1 blocks are physically located in alternating or interleaved fashion.

To shed further light on the enablement of the claims, Appellant points out that banks 0 and 1 are not directly connected. They are connected through the sense amplifiers (346, 340, etc.). Applicant offers the following information to show how the specification defines and uses the word "bank" and "alternating."

Description / Definition of a Memory Bank

The term memory bank is well known to those skilled in the art. An explanation and definition of a memory bank can be found in Applicant's specification on page 15 through 29:

> DRDRAMs, like most commercially available memories, include memory cells that are arranged in rows and columns. Unlike many commercially available memories, however, DRDRAMs are multi-bank devices that have memory cells logically arranged into banks that can be independently accessed. This results in multiple banks within each DRDRAM, each including a number of memory cells. Gathering the memory cells into banks, and allowing different banks to undergo separate operations simultaneously, increases the overall data transfer rate of the device.
>
> Each bank is associated with one or more sense amplifiers that function to read data from, and write data to, the memory cells within the bank. The sense amplifiers serve as a data communications bridge between the banks of memory cells and the data buses external to the

> device. Banks are separately activated, possibly simultaneously, or overlapping in time, prior to a read or write operation. When a bank is activated, it communicates with one or more sense amplifiers. When the read or write operation is complete, the bank is deactivated, and the sense amplifiers are precharged, which readies the sense amplifiers for another operation.

Thus, a bank is a group of memory cells that are activated together. For example, all of the memory cells of Bank 0 are activated at the same time regardless if the memory cells of the bank are spread out across a wide area of the memory device. By having a second memory bank, such as Bank 1, a memory device can activate Bank 0 independent of Bank 1. The prior art shown in Figure 1 uses memory banks but does not utilize the sense amplifiers and the memory banks in an efficient way. Applicant's invention shown in Figure 3 optimizes the use of the memory banks and sense amplifiers.

Description / Definition of Interleave and Alternate

The terms "interleave" and "alternate" are used in the specification to show how the rows of memory cells can have only two banks in each row and get better memory access with this design. The words "interleave" and "alternate" are well known to those skilled in the art and are used in the specification consistent with the normal and usual meanings. Interleave is to place one thing between another, and alternate means a choice between two choices. An explanation and definition of the words "interleave" and "alternate" can be found in Applicant's specification on page 5, lines 19 – 29:

> Figure 3 shows a multi-bank memory device in accordance with the present invention. Memory device 300 includes memory cells arranged in rows and columns. Each column is shown as a vertical strip of memory cells, and each row is shown as a horizontal strip of memory cells. For example, strip 302 is a column that includes memory cells 320, 324, and 328, and strip 370 is a row that includes memory cells 320 and 330. As shown in Figure 1, memory device 100 is arranged into "n" banks labeled Bank 0 through Bank (n-1).
>
> Each row in memory device 300 includes memory cores from two banks interleaved together. For example, strip 370 includes memory cores from Bank 0 and Bank 1 **alternating** across the strip. Also for example, strip 372 includes memory cores from Bank **2 interleaved** with memory cores from Bank 3.

Thus, from the foregoing, one can see that the banks in each row in Fig. 3 are interleaved in an alternating fashion between memory cells of Bank 0 and memory cells of Bank 1.

Therefore, Appellant submits that FIG. 3 does provide adequate enablement for claims 1-12 and 14-60. Thus, Appellant respectfully requests allowance of claims 1-12 and 14-60 over the 35 U.S.C. § 112, first paragraph rejection as these claims are clearly supported by FIG. 3, and throughout the remainder of the specification and figures.

C. Claims 1-12 and 14-60 are patentable over Appellants prior art FIG. 1.

Claims 1-12 and 14-60 were rejected under 35 USC § 103(a) as allegedly being unpatentable over Applicant's Fig. 1 (attached as Exhibit A) which is designated as Prior Art. Appellant respectfully traverses this rejection.

First, however, Appellant respectfully notes that this obviousness rejection under 35 U.S.C. § 103(a) cites only one reference to support the rejection. Despite previous requests for further references in support of this rejection in accordance with M.P.E.P. § 2144.03, no second reference has been provided to show the elements missing from Appellant's Fig. 1. Appellant therefore assumes that the Examiner is taking Official Notice of elements in the claims (such as "interleaving" or "interleaved") which are not found in the single reference cited. Appellant respectfully reiterates the previous traversal this Official Notice and resubmits the previous request for either 1.) cited references in support of this position pursuant to M.P.E.P. § 2144.03, or 2.) submission an Examiner's affidavit as required by 37 C.F.R. § 1.104(d)(2) to support this position.

Second, Appellant respectfully submits that that claims 1-12 and 14-60 are distinguished over the admitted prior art of FIG. 1. Appellant respectfully asserts that a simple comparison to the "Applicant's Fig. 1 Prior Art" to the claims supports the patentability of the claims.

For example, claim 1 recites in part:

> ". . . a first one of the first strips including all memory core blocks from a first memory bank and all memory core blocks from a second memory bank, the memory core blocks from the first and second banks being interleaved in the first one of the first strips row in an alternating fashion; . . . ."

In contrast, Appellant cannot find in FIG. 1, or its description, any disclosure, teaching, or suggestion of, among other things, a first one of the first strips including all memory core blocks from a first memory bank and all memory core blocks from a second memory bank, the memory core blocks from the first and second banks being interleaved in the first one of the first strips in an alternating fashion. Instead, Fig. 1 shows rows with only one memory core block from each bank, with other memory core blocks from the same bank being in different rows. Moreover, Fig. 1 does not show interleaving in an alternating fashion, as discussed above. Accordingly, Applicant respectfully requests withdrawal of this basis of rejection of these claims.

Further, FIG. 3 is one example embodiment that includes elements of the present claims. Comparing FIG. 3 to FIG. 1 highlights a difference between the claimed subject matter the admitted prior art. For example, the top row of FIG. 1 illustrates, from right-to-left, memory core blocks from Bank 0, Bank 1, Bank 2, Bank 3, Bank 4, . . . , up to Bank (n-1) – that is, the Banks are not interleaved in alternating fashion in FIG. 1. In contrast, the top row of FIG. 3, from right-to-left, illustrates Bank 0, Bank 1, Bank 0, Bank 1, Bank 0, Bank 1, etc. memory core blocks interleaved in alternating fashion. Additionally, no row in FIG. 1 includes at least two memory cores from the same memory bank. Additionally, no row ("strip") in FIG. 1 includes "all of the all memory core blocks from a first memory bank and all memory core blocks from a second memory bank" as claimed. Therefore FIG. 1 cannot obtain an alternating or interleaved arrangement.

Thus, Appellant respectfully submits that claims 1-12 and 14-60 are patentable because each claim includes some or all of the elements discussed above which FIG. 1 fails to teach or suggest.

For example, independent claim 5 recites in part, ". . . wherein the memory cores in a first one of the first strips are arranged in an *alternating* fashion of two different banks. . . ." (*emphasis* added). Further, independent claim 9 recites in part, ". . . a second bank of memory cores *interleaved* in the linear strip with memory cores of the first bank . . . the strip comprising *only* those memory cores from the first and second banks." (*emphasis* added).

Another example include independent claim 14 which recites in part, ". . . a second bank of memory cores *interleaved* with the first bank of memory cores arranged in the strip that includes *all* of the memory cores in the second bank . . . ." (*emphasis* added). Yet further, independent claim 18 recites in part, ". . . wherein a strip of memory cores in the first dimension includes *all* of the memory cores from a first bank *interleaved* with *all* of the memory cores from a second bank . . . ." (*emphasis* added).

The remaining claims include similar elements providing for alternating and/or interleaved memory core blocks in strips/dimensions/rows. FIG. 1 fails to teach or suggest alternating memory banks in a strip and interleaving memory core blocks from a bank in an alternating fashion across a strip as claimed.

Reversal of the 35 U.S.C. § 103(a) rejection and allowance of claims 1-12 and 14-60 is earnestly requested.

D. Drawing Objections

The Final Office Action in paragraph 1 on page 2 objects to the drawings for allegedly failing to show every feature of the invention specified in the claims. The Final Office Action asserts that "the first and second banks interleaved in each row in an alternating fashion" is not illustrated in the figures. However, Appellant refers the Board's attention to FIG. 3. Further, for the sake of brevity, Appellant further refers the Board's attention to the portion of the argument above with regard to the Section 112 rejection under the subheading "Description/Definition of Interleave and Alternate." FIG. 3 illustrates the interleaving and the referenced portion of the argument provides further insight. Appellant respectfully submits that FIG. 3 illustrates the elements the Examiner asserts are missing.

8. SUMMARY

For the reasons argued above, Appellant respectfully submits that claims 1-12 and 14-60 are enabled and are patentable. Reversal of the claim rejections and allowance are earnestly requested.

Respectfully submitted,

BRIAN M. SHIRLEY et al.

By their Representatives,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Appeal Brief, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 30 day of November, 2005.

KATE GAINOR _____
Name Signature

CLAIMS APPENDIX

1. (Rejected) A memory device comprising:

a plurality of banks, each bank including a plurality of memory core blocks that are selected for activation or deactivation together, the memory core blocks arranged in a plurality of first strips and second strips, the second strips orthogonal to the first strips, a first one of the first strips including all memory core blocks from a first memory bank and all memory core blocks from a second memory bank, the memory core blocks from the first and second banks being interleaved in the first one of the first strips row in an alternating fashion; and

a plurality of sense amplifiers shared between and interleaved, in the first one of the first strips, with the memory core blocks of the first and second memory banks.

2. (Rejected) The memory device of claim 1 wherein column decode conductors traverse the memory core blocks in the first one of the first strips.

3. (Rejected) The memory device of claim 2 further comprising sense nodes substantially parallel to the column decode conductors.

4. (Rejected) The memory device of claim 1 wherein each one of the first strips interleaves all memory core blocks from two different banks.

5. (Rejected) A memory device comprising:

a plurality of memory cores logically arranged into a plurality of banks, each bank selectably activating or deactivating its memory cores together as a group, with each memory core assigned to a unique one of the memory banks, and the memory cores are arranged into a plurality of first strips and second strips, wherein the second strips are orthogonal to the first strips, and with each memory core in a first one of the second strips being associated with a different one of the banks;

a plurality of sense amplifiers, each sense amplifier being shared between two unique memory cores in a first one of the first strips, wherein the two unique memory cores are from different banks; and

wherein the memory cores in a first one of the first strips are arranged in an alternating fashion of two different banks with a sense amplifier between adjacent memory cores in the first one of the first strips.

6. (Rejected) The memory device of claim 5 further comprising column decode conductors for the first one of the first strips, the column decode conductors for the first one of the first strips being coupled to all the sense amplifiers in the first one of the first strips.

7. (Rejected) The memory device of claim 5 wherein the first one of the first strips includes all memory cores from a first one of the banks.

8. (Rejected) The memory device of claim 5 wherein the first one of the first strips includes all memory cores from a first one of the banks and all memory cores from a second one of the banks.

9. (Rejected) A memory device comprising:

a first bank of memory cores arranged in a linear strip and selectable for activation and deactivation together as a first group;

a second bank of memory cores interleaved in the linear strip with memory cores of the first bank, the second bank of memory cores selectable for activation and deactivation together as a second group; and

a plurality of sense amplifiers shared between memory cores of the first bank and memory cores of the second bank along the linear strip, the strip comprising only those memory cores from the first and second banks.

10. (Rejected) The memory device of claim 9 further comprising a plurality of memory cores arranged as horizontal strips and a plurality of memory cores of vertical strips arranged perpendicular to the horizontal strips, wherein the linear strip is one of the plurality of horizontal strips.

11. (Rejected) The memory device of claim 10 wherein each of the plurality of horizontal strips includes interleaved memory cores from two different banks.

12. (Rejected) The memory device of claim 9 wherein each of the plurality of sense amplifiers is coupled to one memory core of the first bank and one memory core of the second bank.

13. (Withdrawn)

14. (Rejected) A memory device comprising:

a first bank of memory cores arranged in a strip that includes all of the memory cores in the first bank, the first bank of memory cores selectable for activation and deactivation together as a first group;

a second bank of memory cores interleaved with the first bank of memory cores arranged in the strip that includes all of the memory cores in the second bank, the second bank of memory cores selectable for activation and deactivation together as a second group independently from the first group;

a plurality of sense amplifiers shared between memory cores of the first bank and memory cores of the second bank; and

a column decoder arranged to drive column decode lines coupled to the plurality of sense amplifiers.

15. (Rejected) The memory device of claim 14 further comprising a plurality of memory cores arranged in horizontal strips and a plurality of memory cores arranged in

vertical strips arranged perpendicular to the horizontal strips, wherein the strip is one of the plurality of horizontal strips.

16. (Rejected) The memory device of claim 15 wherein each of the plurality of horizontal strips includes interleaved memory cores from only two different banks.

17. (Rejected) The memory device of claim 14 wherein each of the plurality of sense amplifiers is coupled to one memory core of the first bank and one memory core of the second bank.

18. (Rejected) An integrated circuit comprising:

an array of memory cores arranged as rows along a first dimension and arranged as columns along a second dimension; and

wherein a strip of memory cores in the first dimension includes all of the memory cores from a first bank interleaved with all of the memory cores from a second bank interspersed with shared sense amplifiers between memory cores of different banks, wherein each particular bank is selectable to activate or deactive all of the memory cores associated with the particular bank.

19. (Rejected) The integrated circuit of claim 18 wherein the first dimension includes a plurality of horizontal strips of memory cores, and the second dimension includes a plurality of vertical strips of memory cores, and each of the plurality of horizontal strips includes interleaved memory cores from two different banks.

20. (Rejected) The integrated circuit of claim 19 wherein each of the plurality of vertical strips includes non-interleaved memory cores from different banks, and each memory core in a particular vertical strip is from a different bank than the other memory cores in that same particular vertical strip.

21. (Rejected) The integrated circuit of claim 18 further comprising:

a column decoder; and

a plurality of column decode conductors driven by the column decoder and situated substantially parallel to the strip of memory cores.

22. (Rejected) An integrated circuit comprising:

an array of memory cores, the array having a first dimension and a second dimension, wherein a strip of memory cores in the first dimension includes all of the memory cores from a first bank interleaved with all of the memory cores from a second bank, wherein each bank is selectable to activate or deactivate all of the memory cores in that bank; and

a plurality of sense amplifiers arranged between memory cores from the first bank and memory cores from the second bank.

23. (Rejected) The integrated circuit of claim 22 wherein:

the first dimension includes a plurality of horizontal strips of memory cores;

the second dimension includes a plurality of vertical strips of memory cores; and

each of the plurality of horizontal strips interleaves all of the memory cores from two different banks.

24. (Rejected) The integrated circuit of claim 23 wherein each of the plurality of vertical strips includes non-interleaved memory cores, and in which each of the non-interleaved memory cores within a particular vertical strip is associated with a different memory bank.

25. (Rejected) The integrated circuit of claim 22 further comprising:

a column decoder; and

a plurality of column decode conductors driven by the column decoder, coupled to the plurality of sense amplifiers, and situated substantially parallel to the strip of memory cores.

26. (Rejected) An integrated circuit comprising:

an array of memory cores having a first dimension and a second dimension, wherein a strip of memory cores in the first dimension includes memory cores from a first bank interleaved with memory cores from a second bank, and in which the strip includes all of the memory cores in the first bank and all of the memory cores in the second bank, an in which each bank is selectable to activate or deactivate all of its memory cores;

a plurality of sense amplifiers arranged between memory cores from the first bank and memory cores from the second bank; and

column decode conductors coupled to the plurality of sense amplifiers, the column decode conductors arranged to be near memory cores of the first and second bank.

27. (Rejected) The integrated circuit of claim 26 wherein the first dimension includes a plurality of horizontal strips of memory cores, and the second dimension includes a plurality of vertical strips of memory cores, and each of the plurality of horizontal strips interleaves all of the memory cores from two different banks.

28. (Rejected) The integrated circuit of claim 27 wherein in each of the plurality of vertical strips, each memory core is from a different bank.

29. (Rejected) A memory device comprising:

a first bank of memory cores that are selectable together as a first group for activation or deactivation;

a second bank of memory cores that are selectable together as a second group for activation or deactivation; and

a plurality of sense amplifiers shared between the first bank of memory cores and the second bank of memory cores;

wherein all of the memory cores in the first bank and all of the memory cores in the second bank are interleaved in a first horizontal strip on the memory device.

30. (Rejected) The memory device of claim 29 further comprising:

a plurality of horizontal strips of which the first horizontal strip is one; and

a plurality of vertical strips of memory cores, each of the plurality of vertical strips of memory cores having non-interleaved memory cores from a plurality of banks.

31. (Rejected) The memory device of claim 29 further comprising:

a third bank of memory cores;

a fourth bank of memory cores;

a plurality of sense amplifiers shared between the third bank of memory cores and the fourth bank of memory cores; and

wherein the third bank of memory cores and the fourth bank of memory cores are interleaved in a second horizontal strip parallel to the first horizontal strip.

32. (Rejected) The memory device of claim 29 further comprising pass transistors coupled to the plurality of sense amplifiers to select data from either the first bank of memory cores or the second bank of memory cores.

33. (Rejected) A memory device comprising:

a first bank of memory cores that are selectable together as a first group for activation or deactivation;

a second bank of memory cores that are selectable together as a second group for activation or deactivation, wherein all of the memory cores of the first bank and all of the memory cores of the second bank are interleaved in a first horizontal strip on the memory device;

a plurality of sense amplifiers shared between the first bank of cores and the second bank of cores;

a column decoder; and

a plurality of column decode conductors coupled to the column decoder and the plurality of sense amplifiers, the plurality of column decode conductors being substantially parallel to the first horizontal strip on the memory device.

34. (Rejected) The memory device of claim 33 further comprising:

a plurality of horizontal strips of which the first horizontal strip is one; and

a plurality of vertical strips of memory cores, each of the memory cores in a particular one of the vertical strips associated with a different bank than the other memory cores in the particular one of the vertical strips.

35. (Rejected) The memory device of claim 33 further comprising:

a third bank of memory cores;

a fourth bank of memory cores; and

a plurality of sense amplifiers shared between the third bank of memory cores and the fourth bank of memory cores;

wherein all of the memory cores in the third bank of memory cores and all of the memory cores in the fourth bank of memory cores are interleaved in a second horizontal strip parallel to the first horizontal strip.

36. (Rejected) A memory device comprising:

a plurality of memory cores physically arranged in horizontal strips and vertical strips and logically arranged into banks that share sense amplifiers, wherein each particular bank is selectable to activate or deactivate all of the memory cores associated with that particular bank, and wherein all of the memory cores arranged in a first horizontal strip alternate between a first bank and a second bank.

37. (Rejected) The memory device of claim 36 further comprising:

a column decoder;

column decode conductors coupled between the column decoder and the sense amplifiers
shared between the first bank and the second bank; and

sense nodes coupled to the sense amplifiers, arranged substantially parallel to the column decode conductors.

38. (Rejected) The memory device of claim 36 wherein all of the memory cores in a second horizontal strip are arranged to alternate between a third bank and a fourth bank.

39. (Rejected) The integrated circuit of claim 36 wherein each of the of vertical strips includes non-interleaved memory cores from different banks.

40. (Rejected) A memory device comprising:

a plurality of memory cores physically arranged in horizontal strips and vertical strips and logically arranged into banks that share sense amplifiers, wherein each particular bank is selectable to activate or deactivate all of the memory cores associated with that particular bank, and wherein all of the memory cores arranged in a first horizontal strip alternate between a first bank and a second bank; and

column decode conductors arranged in the first horizontal strip to cross memory cores from only the first bank and the second bank.

41. (Rejected) The memory device of claim 40 further comprising:

a second horizontal strip having interleaved all of the memory cores from a third bank and a fourth bank; and

a second plurality of sense amplifiers shared between the third bank and the fourth bank.

42. (Rejected) The memory device of claim 40 wherein each of the vertical strips includes non-interleaved memory cores that are taken only from different banks.

43. (Rejected) A memory device comprising:

a plurality of memory cores physically arranged in a plurality of horizontal strips and a plurality of vertical strips and logically arranged into banks, wherein each particular bank is selectable to activate or deactivate all of the memory cores associated with that particular bank; and

wherein each horizontal strip interleaves in alternating fashion all memory cores from only two of the banks, and no two memory cores in any particular vertical strip is from the same bank.

44. (Rejected) The memory device of claim 43 further comprising sense amplifiers shared between memory cores in each of the plurality of horizontal strips.

45. (Rejected) The memory device of claim 44 further comprising column decode conductors dedicated to each horizontal strip, each column decoder conductor passing over memory cores of two banks and no more.

46. (Rejected) A computer system comprising:

a processor; and

a memory device coupled to the processor, the memory device including:

a plurality of horizontal strips and vertical strips of memory cores; and

a plurality of sense amplifiers positioned between memory cores within each horizontal strip, wherein every memory core is associated with a particular bank that is selectable to activate or deactivate all of the memory cores associated with that particular bank, and wherein only every other memory core within a first horizontal strip is assigned to a the same bank, and wherein each of the memory cores in the first horizontal strip are associated with one of only two of the banks, and in which two of the banks are represented by memory cores in the first horizontal strip.

47. (Rejected) The computer system of claim 46 wherein each sense amplifier is shared between two banks.

48. (Rejected) The computer system of claim 46 further comprising a memory controller coupled to the processor and the memory device.

49. (Rejected) A computer system comprising:

a processor; and

a memory device coupled to the processor, the memory device including:

a first bank of memory cores arranged in a first horizontal strip, wherein the memory cores of first bank are selectable together as a first group for activation or deactivation;

a second bank of memory cores interleaved with the first bank of memory cores in the first horizontal strip, wherein the memory cores of second bank are selectable together as a second group for activation or deactivation, and wherein all of the memory cores in the first and second banks are located in the first horizontal strip;

a third bank of memory cores arranged in a second horizontal strip, wherein the memory cores of third bank are selectable together as a third group for activation or deactivation; and

a fourth bank of memory cores interleaved with the third bank of memory cores in the second horizontal strip, wherein the memory cores of fourth bank are selectable together as a fourth group for activation or deactivation, and wherein all of the memory cores in the third and fourth banks are located in the second horizontal strip.

50. (Rejected) The computer system of claim 49 wherein the memory device further includes:

a first plurality of sense amplifiers shared between the first bank of memory cores and the second bank of memory cores; and

a second plurality of sense amplifiers shared between the third bank of memory cores and the fourth bank of memory cores.

51. (Rejected) The computer system of claim 49 further comprising a memory controller coupled to the processor and the memory device.

52. (Rejected) A computer system comprising:

a processor; and

a memory coupled to the processor, the memory including:

a plurality of sense amplifiers;

a first bank of memory cores, each coupled to at least one of the plurality of sense amplifiers, wherein the memory cores of first bank are selectable together as a first group for activation or deactivation; and

a second bank of memory cores, each coupled to at least one of the plurality of sense amplifiers, wherein the memory cores of second bank are selectable together as a second group for activation or deactivation;

wherein all of the memory cores of the first bank and all of the memory cores of the second bank are arranged in a strip with the plurality of sense amplifiers.

53. (Rejected) The computer system of claim 52 wherein the memory further includes:

column decode conductors coupled to the plurality of sense amplifiers and

a column decoder to drive the column decode conductors.

54. (Rejected) The computer system of claim 52 further comprising a memory controller coupled to the processor and the memory device.

55. (Rejected) A computer system comprising:

a processor;

a memory controller coupled to the processor; and

a memory device coupled to the memory controller, the memory device including:

a plurality of memory cores logically arranged into Rambus-compatible banks, wherein each particular bank is selectable to activate or deactivate all of the memory cores associated with that particular bank, and physically arranged into horizontal strips and vertical strips, wherein each vertical strip interleaves all of the memory cores from two different Rambus-compatible banks.

56. (Rejected) The computer system of claim 55 wherein the memory device includes sense amplifiers shared between memory cores of Rambus-compatible banks in each horizontal strip.

57. (Rejected) A multibank memory device allowing simultaneous access of some of a plurality of memory banks while suffering reduced noise in sense amplifiers, the memory device comprising:

a plurality of memory banks, each memory bank including a plurality of memory cores, the memory cores arranged in strips of comprising horizontal strips and vertical strips, wherein each particular bank is selectable to activate or deactivate all of the memory cores associated with that particular bank;

a plurality of sense amplifiers shared among the memory cores of different ones of the plurality of memory banks;

a plurality of column decoders, each column decoder exclusively accessing a horizontal strip of all of the memory cores from only two of the memory banks wherein the memory cores are separated from each other in the horizontal strip by shared sense amplifiers whereby the memory cores of the horizontal strip alternate between the two memory banks.

58. (Rejected) A memory architecture having n memory banks which allows simultaneous access of some of the memory banks, each memory bank including a plurality of memory cores, wherein each particular bank is selectable to activate or deactivate all of the memory cores associated with that particular bank, the memory cores arranged in horizontal strips, each horizontal strip having an associated column decoder connected to each memory core of the horizontal strip and each core of the horizontal strip associated with only one of only two memory banks.

59. (Rejected) A multibank memory architecture allowing simultaneous access of some of a plurality of memory banks while suffering reduced noise in sense amplifiers, the memory architecture comprising:

a plurality of memory banks, each memory bank containing a plurality of memory cores, wherein each bank is selectable to activate or deactivate all of its associated memory cores, the memory cores arranged in strips, each strip containing all memory cores of only two memory banks and the strip having cores arranged to be alternating between the two memory banks with sense amplifiers shared between the cores of the two memory banks.

60. (Rejected) A multibank memory architecture allowing simultaneous access of some of a plurality of memory banks, the memory architecture comprising a horizontal strip of all of the memory cores from only two of the memory banks interspersed between shared sense amplifiers, each memory core being a part of one of N memory banks, wherein each bank is selectable to activate or deactivate all of its associated memory cores, the strip having the memory cores laid out so that no two memory cores of the same memory bank share a common sense amplifier.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.

EXHIBIT A

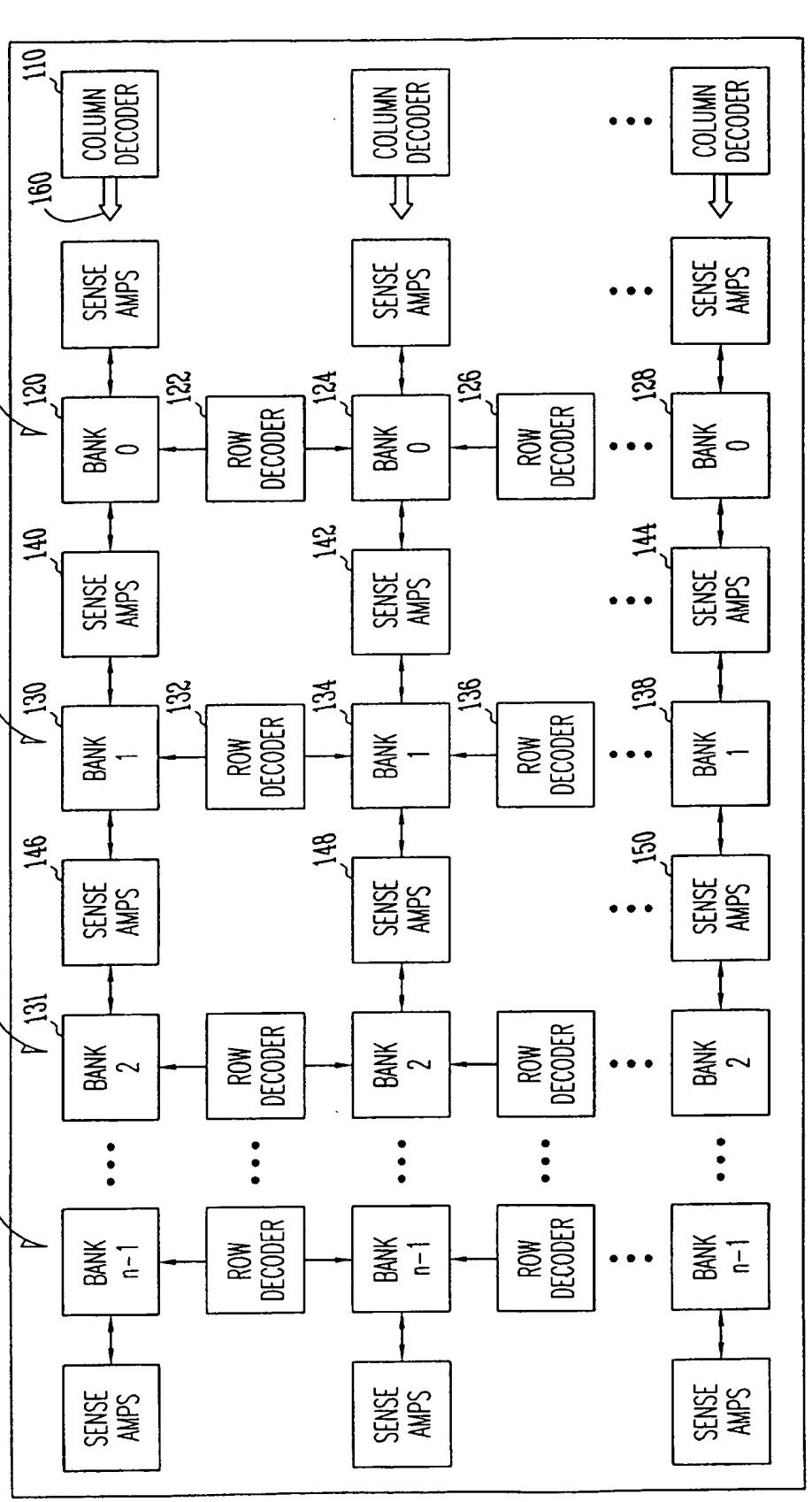

Fig. 1 (Prior Art)

ANNOTATED SHEET SHOWING CHANGES

S/N 09/809,586
Filed March 15, 2001

EXHIBIT B

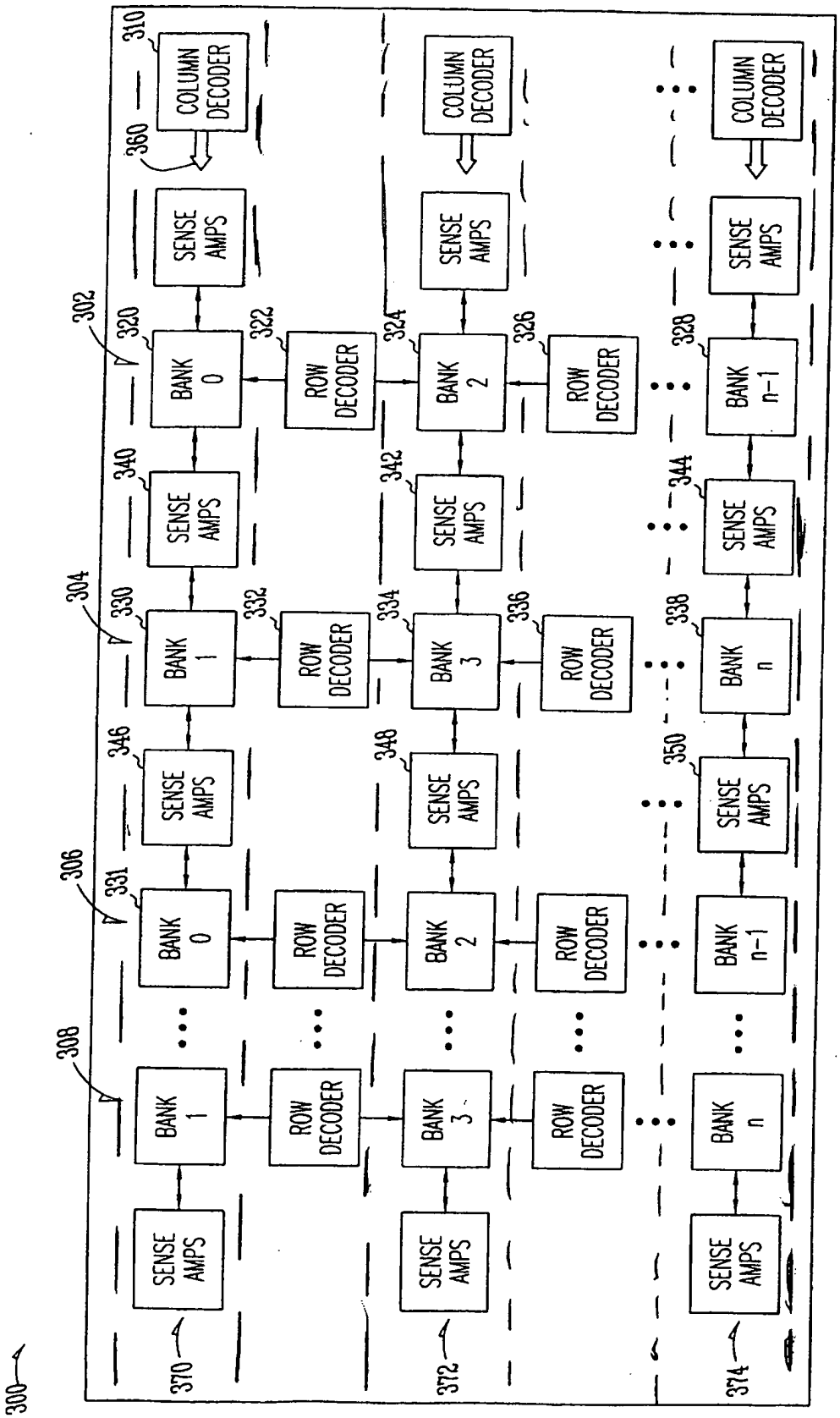

Fig. 3